UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,060	06/27/2003	Kurt D. Beigel	96-0755.20	8492

7590 02/18/2004

Charles Brantley
Micron Technology, Inc.
8000 S Federal Way
Boise, ID 83716

EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/608,060	BEIGEL ET AL.	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *56,73,74 and 139-149* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *74,139-141 and 143-148* is/are allowed.

6)☒ Claim(s) *56,74,142 and 149* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 56, 73, 142 and 149 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (5,748,544).

3. With respect to claim 56, Hashimoto (Fig.3) discloses a method of regulating a control device (precharge and sense circuit) within a semiconductor device, comprising: driving said control device (precharge and sense circuit) with a first voltage (Vref from external source); performing a first operation (testing operation) on said semiconductor device; driving said control device with a second voltage (Vref from generator); and

performing a second operation (normal operation) on said semiconductor device (see col. 3, lines 32-64).

4. With respect to claim 73, Hashimoto (Fig.3) discloses a voltage regulator (3, 30, 31, 32, 33) for a memory circuit including an equilibration device (15, 16, 17), a digit line pair (BITLINE, BITLINE_), and a memory cell, comprising; a voltage reception device (31, 32, 33) comprising a first terminal, a second terminal (3), and a third terminal (test signal terminal), wherein: said voltage reception device is configured to couple to said memory cell by way of said first terminal (one of two terminals receiving EXT Vref and voltage from Vref generator unit), said equilibration device and at least one line of said digit line pair, and wherein said voltage reception device is further configured to couple to an equilibration voltage at said second terminal (3); said voltage reception device is selectively coupled to a first test voltage (Test Signal) at said third terminal; and said voltage reception device is configured to allow a signal transmission between said first terminal and said second terminal in response to a voltage applied to said third terminal (test signal terminal).

5. With respect to claim 142, Hashimoto (Fig.3) discloses a method of regulating a control device (3, 30, 31, 32, 33) for complementary data lines (BITLINE, BITLINE_) within a semiconductor device, comprising: amplifying a voltage difference (by sense amplifier 9) between said complementary data lines using said control device being driven at a first voltage (EXT Vref); and amplifying a voltage difference between said complementary data lines using said control device being driven at a second voltage (Vref generator).

6. With respect to claim 149, Hashimoto (Fig.3) discloses a method of regulating a control device (3, 30, 31, 32, 33) within a semiconductor device, comprising: performing a first read operation on said semiconductor device; driving a read control device (3, 30, 31, 32, 33) with a first voltage (Vref generator) during said step of performing a first read operation; performing a second read operation on said semiconductor device; and driving said read control device with a second voltage (EXT Vref) during said step of performing a second read operation.

7. Claim 56 is rejected under 35 U.S.C. 102(b) as being anticipated by Van Burkirk et al (5,477,499).

8. Van Burkirk et al (Fig.3) disclose a method of regulating a control device (bit line control circuit 320) within a semiconductor device, comprising: driving said control device (bit line control circuit 320) with a first voltage (V program); performing a first operation (programming operation) on said semiconductor device; driving said control device with a second voltage (V read); and performing a second operation (read operation) on said semiconductor device.

9. Claim 56 is rejected under 35 U.S.C. 102(b) as being anticipated by Tada et al (5,297,101).

10. Tada et al (Figures.1-2) disclose a method of regulating a control device (sense circuit 15) within a semiconductor device, comprising: driving said control device (sense circuit 15) with a first voltage (normal voltage with transistor Tr being OFF); performing a

first operation (read operation) on said semiconductor device; driving said control device with a second voltage (test voltage with transistor Tr being ON); and performing a second operation (marginal test operation) on said semiconductor device (see col. 5).

11. Claim 56 is rejected under 35 U.S.C. 102(b) as being anticipated by Petschauer et al (5,361,232).

12. Petschauer et al (Fig.2) disclose a method of regulating a control device (sense circuit) within a semiconductor device, comprising: driving said control device (sense circuit) with a first voltage (normal voltage with transistor 24 and 26 being ON); performing a first operation (read operation) on said semiconductor device; driving said control device with a second voltage (test voltage with transistor 24 and 26 being OFF); and performing a second operation (test operation) on said semiconductor device (see col. 4)

Allowable Subject Matter

13. Claims 74, 139-141, 143-148 are allowed.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

15. Lee et al (5,590,079) disclose a wafer burn-in test circuit for a memory device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571)272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571)-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le
Primary Examiner
Art Unit 2824

02/12/04